CLAIMS

Having thus described our invention, what we claim as new and desire to secure by Letters Patent is as follows:

1. A method of applying transforms for simultaneously modifying a plurality of domains, including at least one of a boolean domain, an electrical domain, and a physical domain, concurrently in a design space, comprising:

selectively applying a set of more and less granular placement and netlist modification transforms separately or in a flexible sequence to create a converging design process flow,

wherein said transforms comprise fine-grained steps to optimize the netlist and placement properties of a design concurrently.

2. The method according to claim 1, wherein said creating starts from a netlist without an initial placement of said circuit on a chip or from a netlist with an initial placement.

3. The method according to claim 1, wherein a function of said placement and synthesis transforms are decomposed into a set of fine-grained transforms each addressing a specific phase of the placement and synthesis process.

4. The method according to claim 3, wherein said placement transforms are selectively mixed and matched with predetermined logic synthesis transforms and fine-grained transforms.

5. The method according to claim 1, wherein a single transform selectively optimizes the physical, boolean and electrical domains, thus moving the design from a start point to an end point in the design space.

6. The method according to claim 1, wherein a single fine-grained transform includes multiple objectives and constraints which involve physical placement and logical data.

7. The method according to claim 1, wherein a partially placed and synthesized design is a starting point of said creating.

8. The method according to claim 1, wherein said design process flow comprises a single converging flow of successive application of fine-grained operations.

9. The method according to claim 1, further comprising utilizing an infrastructure of bins, and wherein a timing, congestion and noise analysis is based on the bins.

10. The method according to claim 1, wherein placement and netlist changes are performed together in said fine-grained transforms.

11. The method according to claim 1, wherein said fine-grained transforms are organized together in flexible scenarios to create a design closure process.

12. The method according to claim 1, further comprising:

at predetermined stages of the process, selectively determining whether to intercept the process and implement any of a plurality of fine-grained transforms.

13. The method according to claim 1, further comprising:

examining a plurality of domains concurrently in finding an optimum design, said examining comprising creating a sequence of more and less granular placement and netlist modification transforms, to create a converging design closure process.

14. The method according to claim 1, wherein all transforms have a unified view of the placement and synthesis design space.

15. The method according to claim 14, wherein synthesis, timing, and placement data are concurrently available to all of said transforms, such that said transforms modify a netlist and placement concurrently.

16. A method of applying fine-grained transformations during placement synthesis interaction, comprising:

(a) creating and updating bins;

(b) applying a plurality of transforms on a bin-based database updated by both placement and synthesis;

(c) updating the bin-based timing, and invoking a synthesis-placement script;

(d) selecting fine-grained synthesis and placement transforms;

(e) invoking selected transforms within said script using a driver; and

(f) applying transforms that change the physical, electrical and boolean logic design space concurrently.

17. The method according to claim 16, further comprising:

repeating (A) through (F) until design convergence.

18. The method according to claim 16, wherein a design space is moved from one point to another by considering concurrently subsets of fine-grained boolean transforms, electrical transforms, and physical transforms.

19. The method according to claim 18, wherein blocks of each of the boolean optimizations, electrical optimizations and physical optimizations are interspersed together.

20. The method according to claim 19, wherein each of said optimizations is represented as a plurality of transformations such that the optimizations are divided and interspersed together, to examine each of the boolean, electrical and physical domains concurrently.

21. A method for applying fine grained transformations during placement synthesis interaction, comprising:

creation and updating of bins;

applying the transforms on a bin-based database updated by both placement and synthesis;

updating the bin-based timing;

invoking a synthesis-placement script based on said placement and said synthesis;

selecting fine-grained synthesis and placement transforms;

invoking selected transforms within said synthesis-placement script;

applying transforms that change the physical, electrical and boolean space concurrently; and

repeating the above until design convergence.

22. A system for applying transforms for modifying a plurality of domains concurrently in a design space, comprising:

a unit for creating a sequence of more and less granular placement and netlist modification transforms to create a converging design process flow,

wherein said transforms are fine-grained transforms allowing selective mixing and matching of said fine-grained transforms to optimize the placement of a circuit in a design space.

23. The system according to claim 22, wherein said unit for creating starts from a netlist without an initial placement of said circuit on a chip or from a netlist with an initial placement.

24. The system according to claim 22, wherein a function of said placement and synthesis transforms are decomposed into a set of fine-grained transforms each addressing a specific phase of the placement and synthesis process.

25. The system according to claim 24, wherein said placement transforms are selectively mixed and matched with predetermined logic synthesis transforms and fine-grained transforms.

26. The system according to claim 22, wherein a single transform selectively optimizes the physical, boolean and electrical domains, thus moving the design from a start point to an end point in the design space.

27. The system according to claim 22, wherein a single fine-grained transform includes multiple objectives and constraints which involve physical placement and logical data.

28. The system according to claim 22, wherein a partially placed and synthesized design is a starting point for said unit for creating.

29. The system according to claim 22, wherein said design process flow comprises a single converging flow of successive application of fine-grained operations.

30. The system according to claim 22, further comprising an infrastructure of bins, and wherein a timing, congestion and noise analysis is based on the bins.

31. The system according to claim 22, wherein placement and netlist changes are performed together in said fine-grained transforms.

32. The system according to claim 22, wherein said fine-grained transforms are organized together in flexible scenarios to create a design closure process.

33. The system according to claim 22, further comprising:

a unit, at predetermined stages of the process, for selectively determining whether to intercept the process and implement any of a plurality of fine-grained transforms.

34. The system according to claim 22, further comprising:

an examining unit for examining a plurality of domains concurrently in finding an optimum design, said examining unit comprising a unit for creating a sequence of more and less granular placement and netlist modification transforms, to create a converging design closure process.

35. The system according to claim 22, wherein all transforms have a unified view of the placement and synthesis design space.

36. The system according to claim 35, wherein synthesis, timing, and placement data are concurrently available to all of said transforms, such that said transforms modify a netlist and placement concurrently.

37. A software system for applying transforms for modifying a plurality of domains concurrently in a design space, comprising:

a module for creating a sequence of more and less granular placement and netlist modification transforms to create a converging design process flow,

wherein said transforms are fine-grained transforms allowing selective mixing and matching of said fine-grained transforms to optimize the placement of a circuit in a design space.

38. A programmable storage medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method of applying transforms for modifying a plurality of domains concurrently in a design space, comprising:

creating a sequence of fine-grained transforms to create a converging design process flow

wherein said fine-grained transforms optimize the boolean, physical and electrical aspects of a design concurrently.

39. A programmable storage medium tangibly embodying a program of machine-readable instructions executable by a digital processing apparatus to perform a method of applying fine-grained transformations during placement synthesis interaction, comprising:

(a) creating and updating bins;

(b) applying a plurality of transforms on a bin-based database updated by both placement and synthesis;

(c) updating the bin-based timing, and invoking a synthesis-placement script;

(d) selecting fine-grained synthesis and placement transforms;

(e) invoking selected transforms within said script using a driver; and

(f) applying transforms that change the physical, electrical and boolean logic design space concurrently.